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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of
JEROEN ANTON JOHAN LEIJTEN

Atty. Docket
NL 010073

Serial No. 10/059,427

Confirmation No. 6839
Group Art Unit: 2183

Filed: JANUARY 29, 2002

Examiner: PETRANEK, J.A.

Title: VARIABLE LENGTH VLIW INSTRUCTION WITH INSTRUCTION FETCH CONTROL BITS FOR PREFETCHING, STALLING, OR REALIGNING IN ORDER TO HANDLE PADDING BITS AND INSTRUCTIONS THAT CROSS MEMORY LINE BOUNDARIES (As Amended)

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Respectfully submitted,

By _____
Dicran Halajian, Reg. 39,703
Attorney for Appellant
November 13, 2006

Enclosure: Appeal Brief
After Final Amendment
Petition to Revive
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APPEAL BRIEF

Sir:

Appellant herewith respectfully presents a Brief on Appeal as follows, having filed a Notice of Appeal on December 22, 2005:

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of record Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA.

RELATED APPEALS AND INTERFERENCES

Appellants and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-9 are pending in this application. Claims 1-9 are rejected in the Final Office Action mailed September 22, 2005. Claims 1-9 are the subject of this appeal.

STATUS OF AMENDMENTS

Appellant is concurrently filing an after final amendment in response to a Final Office Action dated September 22, 2005, that includes a Replacement Sheet with corrected FIG 2 and a Declaration that does not have any missing letters in the inventor's name and address. This Appeal Brief is in response to the Final Office Action mailed September 22, 2005, that finally rejected Claims 1-9.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention, for example, as claimed in independent Claims 1 and 8, where illustrative embodiments are shown in FIGs 1-4, includes a computer system with a processing unit 34 and a memory 30 shown in FIG 3 and described on page 6, lines 23-25. The processing unit 34 is arranged to fetch memory lines from the memory 30 and execute instructions from the memory lines, where FIG 2 shows six illustrative memory lines having a total of nine instructions stored therein, as described on page 9, lines 29-31. Each memory line is fetched as a whole and is capable of holding more than one instruction.

At least one instruction includes information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, such as stall, realign and prefetch bits, as shown in FIG 2, and described on page 11, lines 25-33, where various implementations of the information are

described on page 12, line 25, to page 14, line 2, for example. The processing unit 34 responds to the information by controlling the part as signaled by the information.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 1, 4 and 6-8 of U.S. Patent Application Serial No. 10/059,427 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,819,058 (Miller);

Whether Claims 2-3 and 9 of U.S. Patent Application Serial No. 10/059,427 are unpatentable under 35 U.S.C. §103(a) over Miller in view of U.S. Patent No. 6,684,319 (Mohamed); and

Whether Claim 5 of U.S. Patent Application Serial No. 10/059,427 is unpatentable under 35 U.S.C. §103(a) over Miller in view of U.S. Patent No. 6,546,478 (Keller).

The Appellant respectfully requests the Board to address the patentability of independent Claims 1 and 8, and further Claims 2-7 and 9 as depending from Claims 1 and 8, based on the requirements of independent Claim 1 and 8. This position is provided for the specific and stated purpose of simplifying the current issues on appeal. However, the Appellant herein specifically reserves the right to argue and address the patentability of Claims 2-7 and 9 at a later date should the separately patentable subject matter of Claims 2-7 and 9 later become an issue. Accordingly, this

limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of independent Claims 1 and 8 is not intended as a waiver of Appellant's right to argue the patentability of the further claims and claim elements at that later time.

ARGUMENT

Independent Claims 1 and 8 are said to be anticipated by Miller.

Miller is directed to a system and method for compressing and decompressing variable length instructions. Column 6, lines 20-52; FIGs 7-8; and column 11, line 58 to column 12, line 9 are cited on page 5 of the Final Office Action to allegedly show "at least one instruction comprising information ... that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line," as recited in independent Claim 1, and similarly recited in independent Claim 8.

Further, on page 5 of the Final Office Action, column 6, lines 53-58 are cited to allegedly show that the information is "inserted at compile time," as recited in independent Claim 1, and similarly recited in independent Claim 8.

It is respectfully submitted that the cited portions of Miller are merely concerned with an addressing system using the proper address. In particular, column 11, line 58 to column 12, line 9

specifically recites:

> the addressing system determines ... IP1, is only 16 bits and the memory do not need to be incremented ... Instruction packet IP1 is then read out of the instruction memory, decompressed and executed. Since IP2 is only 48-bits long, the addressing system does not increment either of the Aright or Aleft addresses and IP2 is read out. The addressing system, however, determines that IP3 crosses the 128-bit boundary, so the Aleft address is incremented by one so that addresses 8,9,10, and 11 may be accessed. Thus, IP3 is read out of locations 6,7,8, and 9. To read out IP3, the data in the second memory is read out first and then the data in the first memory is read out. (Emphasis added)

Further, column 6, lines 53-58 merely recites that a word is compressed by a compiler. In particular, column 6, lines 53-58 specifically recites:

> FIG. 4 is a diagram of an uncompressed very long instruction word (VLIW) 120, and a corresponding compressed instruction packet 121 in accordance with the invention. The very long instruction word 120, may be compressed, in accordance with the invention, by a compiler or an assembler. (Emphasis added)

It is respectfully submitted that Miller, such as the word shown in FIG. 4, does not teach or suggest the present invention as recited in independent Claim 1, and similarly recited in

independent Claim 8 which, amongst other patentable elements, requires (illustrative emphasis provided):

> at least one instruction comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line.

Information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary are nowhere taught or suggested in Miller. Accordingly, it is respectfully submitted that independent Claims 1 and 8 is allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that Claims 2-7 and 9 should also be allowed at least based on their dependence from independent Claim 1 and 8.

In addition, Appellant denies any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the

presented remarks. However, the Appellant reserves the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

CONCLUSION

Claims 1-9 are patentable Miller.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
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November 13, 2006

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CLAIMS APPENDIX

1. (Previously Presented) A computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines, each memory line being fetched as a whole and being capable of holding more than one instruction, at least one instruction comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, the processing unit being arranged to respond to the information by controlling said part as signaled by the information.

2. (Original) A computer system according to claim 1, wherein the information signals explicitly whether or not the subsequent memory line has to be prefetched during processing of the instruction, the processing unit being arranged to start

prefetching of the subsequent memory line in response to the information.

3.(Original) A computer system according to Claim 2, wherein the information contains a prefetch bit whose value signals explicitly whether or not the subsequent memory line has to be prefetched.

4.(Original) A computer system according to claim 1, wherein the information signals explicitly whether or not an instruction pointer should be updated form a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information

5.(Original) A computer system according to claim 1, wherein the information signals explicitly whether or not processing of the

instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

6.(Original) A computer system according to Claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to the functional units, the instructions being VLIW instructions, capable of containing two or more operations, the instruction comprising a field distinct from the operations to specify said information.

7.(Original) A computer system according to Claim 6, the field comprising, in addition to said information, a decompression code that specifies for which issue slots the instruction contains operations.

8. (Previously Presented) A method of processing instructions in a computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines capable of holding more than one instruction, at least one instruction comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, the method comprising fetching each memory line as a whole, processing an instruction from a current memory line, reading the information from the instruction during processing and controlling said part as signaled by the information.

9. (Original) A method according to claim 8, wherein said controlling comprises at least one of causing a subsequent memory line to be prefetched or a program counter to skip to a start of the subsequent memory line or processing to be stalled when the

instruction is reached as a branch target.

Claims 10-15 (Canceled)

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None